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ATTY DOCKET NO. POU920030173US1	SERIAL NO. 10/753 852 UNKNOWN
APPLICANT(S) RICH ET AL.	
FILING DATE 1/8/04 HEREWITH	GROUP 2825 UNKNOWN

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
VS	AA	5,349,587	09/20/94	Nadeau-Dostie et al.	371	22.3	
	AB	5,680,543	10/21/97	Bhawmik	395	183.06	
	AC	5,900,753	05/04/99	Cote et al.	327	145	
	AD	5,909,451	06/01/99	Lach et al.	371	22.31	
	AE	6,115,827	09/05/00	Nadeau-Dostie et al.	713	503	
	AF	6,163,545	12/19/00	Flood et al.	370	465	
	AG	6,247,082	06/12/01	Lo et al.	710	105	
	AH	6,327,684	12/04/01	Nadeau-Dostie et al.	714	731	
	AI	6,327,685	12/04/01	Koprowski et al.	714	733	
	AJ	6,434,733	08/13/02	Duggirala et al.	716	11	
	AK	6,442,722	08/27/02	Nadeau-Dostie et al.	714	731	
VS	AL	6,467,044	10/15/02	Lackey	713	501	

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION		
							NO	YES	ABSTRACT
VS	AM	WO 02/077656 A1	03/10/02	EPO	G01R	31/28	X		Yes

OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*

VS	AN	Schmid, et al., "Advanced Synchronous Scan Test Methodology for Multi Clock Domain ASICs", Proceedings 17th, IEEE VLSI Test Symposium, pgs. 106-113, 1999.
VS	AO	IBM Technical Disclosure Bulletin, "Method and Apparatus for Handling Multiple Clock Domain at Speed Logic Built-in Self-Test within a Single Logic Built-in Self-Test Structure", Vol. 38, No. 11, November 1995, pgs. 499 (500)

EXAMINER VUTHE SIEK	DATE CONSIDERED 7/27/06

EXAMINER: Initial here if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. **Include copy of this form with next communication to applicant.**